"selectively growing a top oxide layer on the bottom oxide layer wherein the top oxide layer is formed on the bottom oxide layer at a faster rate than on non-oxide materials." As discussed, for example, at col. 4, line 64 to col. 5, line 9 of Knorr, a high density plasma chemical vapor deposition (HDP-CVD) process is used to deposit the second insulating material 126 as shown in Figure 5 therein. In contrast to Knorr, the amended independent claims recite **selectively growing a top oxide layer on the bottom oxide layer**, which Applicants respectfully submit is not disclosed by an HCP-CVD process as the selective growth is provided via **a reaction with the base material (*i.e.*, the bottom oxide layer)**, not by depositing material. Chen also does not disclose or suggest these recitations.

Furthermore, Knorr does not disclose or suggest, at least, "etching back the bottom oxide layer inside an opening in the gap to expose the upper surface of the pattern"... wherein the upper surface of the pattern comprises "a non-oxide layer" as recited in independent Claim 9. In particular, Figures 3-8 of Knorr show that the first insulating layer 116 is maintained inside the trench 111 and, therefore, is not removed to expose a non-oxide layer. In other words, the first insulating layer 116 is not removed outside the trench 111 to expose a non-oxide layer. To the contrary, the first insulating layer 116 is maintained outside the trench 111 so that any non-oxide layer (such as layer 125) remains covered, and is not exposed.

Furthermore, even assuming for the sake of argument that Chen could somehow disclose "etching back the bottom oxide layer inside an opening in the gap to expose the upper surface... comprising a non-oxide layer," Chen teaches away from the combination, as Knorr states that the first insulator layer 116 should be maintained:

> Because the sequence of insulating material layer 116/126/130 HDP-CVD deposition in the trench 111 and the etch processes to remove the insulating material 116/126/130 from the isolation trench 111 sidewalls results in complete gapfill, there is no possibility of conductive or contaminating materials such as from gate poly-Si or CMP slurry becoming lodged within the isolation trenches 11, creating shorts or defects. *Knorr column 5, lines 55-62.*

As shown above by the cited passage from Knorr, the insulating material 116 is described as an integral part of how isolation trenches 111 are structured to **prevent** shorts or defects. In contrast, Chen shows (for example in Figure 5) that the oxide layer 130 therein is removed from the substrate 100, which is at odds with the discussion in Knorr (where the insulator must be maintained outside the trench). Such removal would appear to defeat the objectives of Knorr, which are reproduced above.

Furthermore, adding the second insulating layer 126 from Knorr to Chen would appear to render the device in Chen inoperative. In particular, Chen discusses the formation of a power MOS device, which calls for the formation of a source/drain layer on the oxide layer 130:

> Therefore, what is needed is to form a bottom oxide layer having a concave surface and the bottom oxide layer is served as an insulating layer of a trench power MOS device. *Chen column 1, lines 65-67.*

> In the conventional technology for fabricating a power MOS device, the power MOS device is fabricated in a trench in a semiconductor substrate and the source/drain regions are fabricated in the trench, too. Before the power MOS device is fabricated in the trench, a bottom oxide layer is firstly formed in the trench. The source/drain regions and the gate are then formed in the trench and the bottom oxide layer is firstly formed in the trench. The source/drain regions and the gate are then formed in the trench and the bottom oxide layer in the trench is served as an insulating layer of the power MOS device. In prior art, the bottom oxide layer is planar and the corner between the bottom oxide layer and the trench has an angle about 90 degrees. Besides, the source or drain region of a trench power MOS is formed on the bottom oxide layer in the trench and a spike effect of the trench power MOS device often occurs on the perpendicular corner between the sidewall oft eh trench and the bottom oxide layer. *Chen column 1, lines 42-57 (portions omitted between the above passages from Chen).*

As shown above, Chen calls for a bottom oxide layer having a concave surface shape. Otherwise, Chen calls for a conventional power MOS device to be formed on the concave bottom oxide, which includes a source/drain region to be formed on the bottom oxide layer. Accordingly, forming a second insulating layer 126 as discussed

in Knorr would render the power MOS device in Chen inoperative as the second insulating layer 126 would not operate as a source/drain region, which is typically formed of a semi-conductor material, not an insulating material as called for in Knorr. Accordingly, combining the structures of Knorr and Chen would appear to render the devices both in Chen and Knorr inoperative. Applicants further submit that dependent Claims 10-15 are patentable over Knorr and Chen for at least the reasons described above in reference to independent Claim 9.

With regard to the rejection of Claim 16, Applicants reiterate that Knorr does not disclose or suggest, at least "forming a bottom oxide layer only at a bottom of a gap in the substrate." In particular, Figures 3-8 show that the first insulating layer 116 is formed both in the trench 111 as well as maintained outside the trench 111.

Furthermore, even assuming for the sake of argument that Chen did somehow disclose or suggest the remaining recitations of independent Claim 16, there is ample evidence of teaching away from a combination of Chen and Knorr for the reasons described above in reference to independent Claim 1. Accordingly, Applicants respectively submit that independent Claim 16 is also patentable over Knorr and Chen for at least the same reasons. Applicants further submit that dependent Claims 4-8 are patentable for at least the reasons described above in reference to independent Claim 16.

CONCLUSION

Applicants have provided a number of reasons herein why Knorr does not disclose or suggest, at least, "etching back the bottom oxide layer inside an opening in the gap to expose the upper surface of the pattern"... wherein the upper surface of the pattern comprises "a non-oxide layer" as recited, for example, in independent Claim 9. Furthermore, Applicants have provided several reasons why Chen and Knorr teach away from a combination with one another and, moreover, how if Chen and Knorr were combined, the conflicting structures called for in each would render the other structure inoperative. Accordingly, Applicants respectfully request withdrawal of all

rejections and the allowance of all claims in due course. If any informal matters arise the Examiner is invited to contact the undersigned by telephone at 919-854-1400.

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Audra Wooten